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EXAMINER	
CRAIG, DWIN M	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/438,856	MEARES, LAWRENCE G.	
	Examiner	Art Unit	
	Dwin M. Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3, 6-12, 15-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7,16 and 37* is/are allowed.

6)☒ Claim(s) *1-3,10-12,19-36 and 40-48* is/are rejected.

7)☒ Claim(s) *6, 8, 9, 15, 17, 18, 38, 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7-29-2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3, 6-12 and 15-39 have been presented for reconsideration based on Applicant's amended claim language and arguments. Claims 40-48 have been presented for Examination. Claims 4, 5, 13 and 14 have been cancelled.

2. Dwin Craig is now the Examiner of record. Eduardo Garcia-Otero is no longer the Examiner of record.

Drawings

3. The Examiner accepts the drawings submitted on 7-29-2005 and any previous objections are hereby withdrawn.

Response to Arguments

4. Applicant's arguments with respect to claims 1-3, 6-12 and 15-39 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-3, 10-12, 19-36 and 40-48 are rejected under 35 USC § 103(a) as being unpatentable over US Patent 5,446,676 Huang et al. in view of US Patent 5,278,769 Bair et al.

5.1 As regards independent claims 1, 10 and 31 and using independent claim 1 as an example, the *Huang et al.* reference discloses,

Adding a first simulation routine to said SPICE netlist to perform a reference simulation of said SPICE netlist to arrive at nominal values for selected vector measurements (Figure 1 items 12, 14, 16 and 18 and Col. 4 line 47 "AS shown in FIG. 1, circuits formatted in a foreign netlist format **10** such as the SPICE(S-P-I-C-E) format should be translated into a native format for simulator **22**. Spice2t." and then Col. 4 line 61, "Aliasfile **16** contains aliases for specified nodes in the SPICE netlist. During translation, names in the SPICE netlist referenced in the aliasfile **16** are *converted* to the alternate name specified in the aliasfile." And Figure 8 items 202. 204, 206, 208), *adding a perturbing routine to said SPICE netlist for altering circuit parameter values of said circuit design in a pre-determined manner;* (Figure 8 item 212, Figure 1 item 34, Figure 9 item 133 "TRANSISTOR PARAMETER RECORD n" and Col. 5 line 2 "Stimulus file **34** contains input data used to stimulate the simulated circuit in simulator **22.** The data or stimuli contained in file **34** may be in a variety of formats, including conventional test *vectors*, simulated clock input, constant period *vector* stimulus specification (stimulus signals to be applied at fixed time intervals) and logical one and zero constants."), *adding a second simulation routine to said SPICE netlist for performing simulations of said circuit design for respective altered circuit*

parameter values to arrive at respective selected vector measurements; and (Figure 1 item 26, 30 and 22 and Table 1, and Col. 9 line 10, "At $\mathbf{V}_s$=0(zero),$\mathbf{V}_t$=**VTO**, which is a SPICE parameter defined for any transistor model. This value may be *adjusted* by control file **24** parameter threholdmos (item 9 of Table 1.)"), *adding an analysis routine to said SPICE netlist for manipulating at least one of said selected vector measurements in accordance with said pre-determined analysis* (Figure 1 item 34 and Col. 13 line 50 "In addition to test vectors, this file contains initialization vectors to set the simulated circuit to a predefined state prior to beginning actual simulation.").

However, the *Huang et al.* reference does not expressly disclose the use of simulation templates.

The *Bair et al.* reference discloses the use of simulation templates (Figure 10 and Col. 7 lines 44-46).

5.2 It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have added the SPICE simulation methods of the *Huang et al.* reference because it becomes extremely desirable to have a method of automating the process so that accurate logic and timing models may be generated quickly (*Bair et al.* Col. 3 lines 46-51), this is also disclosed in the *Huang et al.* reference (Col. 7 lines 6-11).

5.3 As regards dependent claims 19, 25 and 34 the *Huang et al.* reference discloses a circuit parameter value of a resistor (Figure 5 Item 118 and Figure 9 and Col. 17 lines 39-44).

5.4 As regards dependent claims 20, 26 and 35 the *Huang et al.* reference discloses voltage measurements (Figure 9b and Col. 11 lines 20-29 and Col. 14 lines 42-59).

5.5 As regards dependent claims 21 and 27 the *Huang et al.* reference discloses current measurement (Figure 20 and Col. 19 lines 65-68, Col. 20 lines 1-5).

5.6 As regards dependent claims 22, 28 and one portion of dependent claim 35 the *Huang et al.* reference discloses determining power dissipation (Title and Abstract).

5.7 As regards dependent claims 23, 29 and 40-48 the *Huang et al.* reference discloses modeling capacitors and resistors (Figure 9 and Figure 17-19 and Col. 17 lines 39-44).

5.8 As regards dependent claims 24 and 30 the *Huang et al.* reference discloses a parameter value being altered (Figure 9, 9B and Col. 9 lines 10-22).

5.9 As regards dependent claim 32 the *Huang et al.* reference does not expressly disclose a template.

The *Bair et al.* reference discloses the use of simulation templates (Figure 10 and Col. 7 lines 44-46).

As regards the motivation for using the teaching of a simulation template please see section 5.2 of this Office Action.

5.10 As regards dependent claims 3 and 12, one of ordinary skill in the art would be motivated to use MPEP § 2144.04(II)(A) Legal Precedent (eliminating element) to remove the save statements to speed the simulation and the saving of memory, there are no unexpected results from this omission, so MPEP 2144.04(II)(B) does not apply.

5.11 As regards dependent claims 2, 11 and 33 the *Huang et al.* reference does not expressly disclose determining tolerances.

The *Bair et al.* reference discloses checking a simulation against predefined tolerances (Col. 6 lines 63-68 and Col. 7 lines 1-2 and Col. 9 lines 51-59), it is also noted by the Examiner

that there are precision components, specifically precision resistors that are commonly used in circuit design and therefore it would be obvious to include these precision components that have a specified tolerance to a circuit design being simulated.

5.12 As regards dependent claim 36 the *Huang et al.* reference discloses an iterative process of determining a parameter value, which inherently teaches only varying one variable at a time (Figure 3).

Allowable Subject Matter

6. **Claims 7, 16** and **37** are allowed.

6.1 The following is an Examiner's reasons for allowance.

As regards independent claim 16, the following limitations in combination with other limitations are neither anticipated nor made obvious by the prior art, *"a sensitivity analysis involving determining a difference between said respective selected vector measurements and said nominal values for said selected vector measurements"* in combination with *"a root summed square analysis"*.

As regards independent claim 16, the following limitations in combination with other limitations are neither anticipated nor made obvious over the prior art, *"a root summed square analysis involving a sum of square difference between said respective selected vector measurements and said nominal value for said selected vector measurements."*

As regards independent claim 37 the following limitations, in combination with other limitations is neither anticipated nor made obvious by the prior art, *"determining a sum of differences between the plurality of altered vector measurements and the nominal vector measurement, squaring the sum of the differences to determine a root summed square (RSS) for*

the vector measurement of the circuit design in response to alterations in the at least one circuit parameter value of the component in the SPICE netlist."

As regards dependent claims 38 the following limitations, in combination other limitations are neither anticipated nor made obvious by the prior art. *"determining a maximum of a first absolute value of the first altered vector measurement less the nominal vector ,measurement and a second absolute value of the second altered vector measurement less the nominal vector measurement to determine an extreme value analysis (EVA) for the vector measurement of the circuit design."* Dependent claim 38 is objected to because it depends upon an allowed base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As regards dependent claim 39 the following limitations, in combination with other limitations, are neither anticipated nor made obvious by the prior art, *"determining a maximum value of the absolute scalar differences to determine a worst case by sensitivity (WCS) for the selected vector measurement of the circuit design"*. Dependent claim 39 is objected to because it depends upon an allowed base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6.2 Dependent claims 6, 8, 9, 15, 17 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6.3 The Examiner notes that, dependent claim 6 expressly claims the limitation of performing a *"sensitivity analysis"* as disclosed in dependent claim 39.

6.4 The Examiner notes that dependent claim 8 expressly claims performing an *"extreme value analysis"* as disclosed in dependent claim 38.

6.5 The Examiner notes that dependent claim 9 expressly claims performing a *"worst case sensitivity analysis"* as disclosed in claim 39.

6.6 The Examiner notes that dependent claim 15 expressly claims a *"sensitivity analysis"* as disclosed in claim 39.

6.7 The Examiner notes that claim 17 expressly claims an *"extreme value analysis"* as disclosed in claim 38.

6.8 The Examiner notes that claim 18 expressly claims a *"worst case sensitivity analysis"* as disclosed by claim 39.

Conclusion

7. Claims 1-3, 6-12 and 15-39 have been presented for reconsideration based on Applicant's amended claim language and arguments. Claims 40-48 have been presented for Examination. Claims 4, 5, 13 and 14 have been cancelled.

7.1 Claims 7, 16 and 37 are allowed. Claims 6, 8, 9, 15, 17, 18, 38 and 39 are objected to. Claims 1-3, 10-12, 19-36 and 40-48 are rejected.

7.2 This Office Action is Non-Final.

7.3 The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent 5,838,947 discloses methods of performing a circuit simulation using a SPICE deck (Figure 7).

US Patent 5,297,066 discloses the use of a SPICE netlist and vector models in a simulator (Figure 1).

US Patent 5, 798,938 discloses the use of SPICE netlists and vectors in a circuit simulation (Col. 3 lines 32-38 and Col. 9 line 4).

US Patent 6,842,727 discloses the sue of extracting circuit component netlist data (Figures 1 and 2).

7.4 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M. Craig whose telephone number is (571) 272-3710. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-830.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC

Paul L. Rodriguez 8/26/05
Primary Examiner
Art Unit 2125